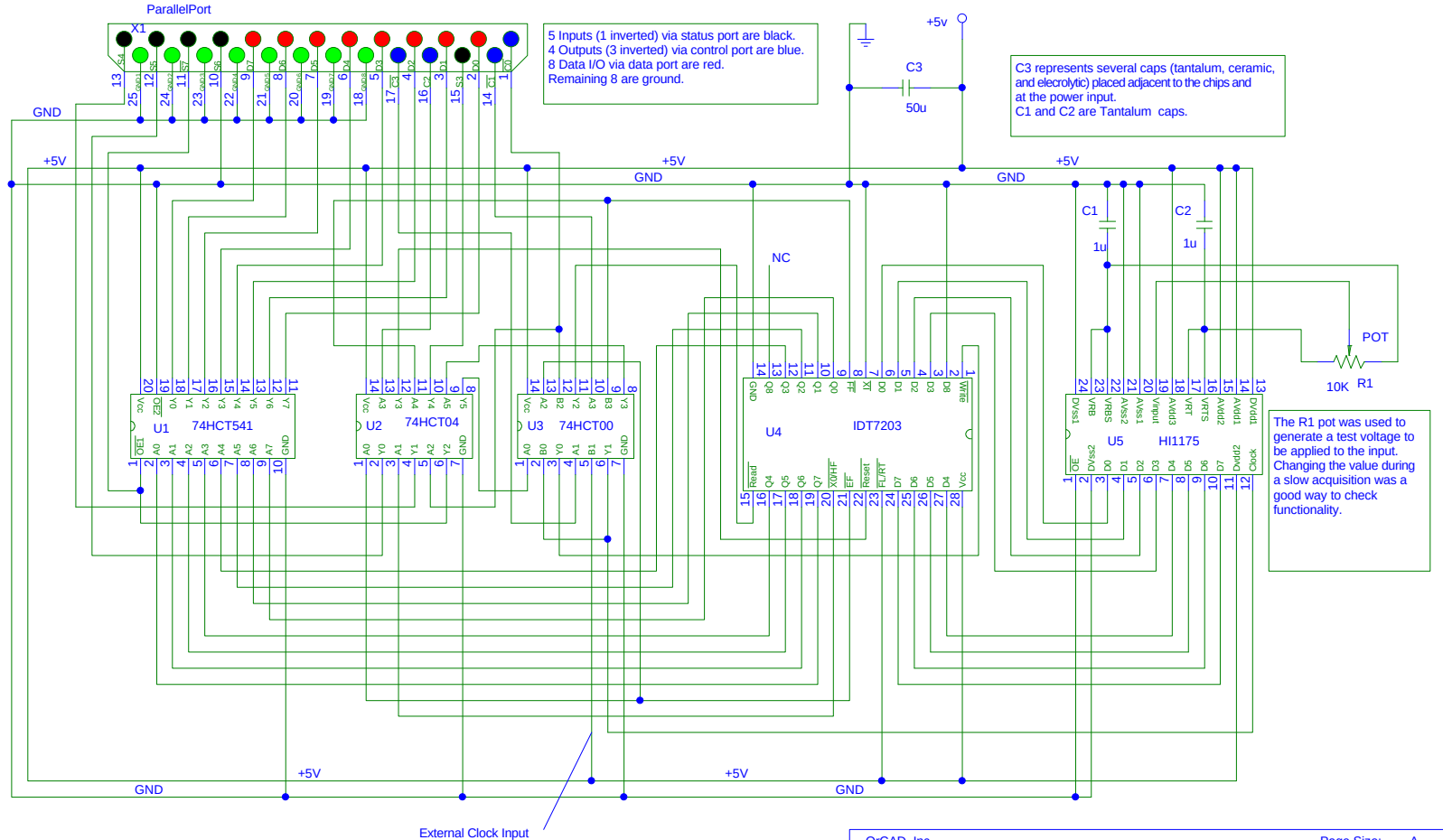
20MHz Parallel Port Oscilloscope: Phase 1

Phase 1:
This is a Proof of Principle setup designed to test the feasibility of a parallel port o'scope made from just a 20MHz A/D and a FIFO (along with some "glue" logic). The IDT7203 and the HI1175 are FREE samples from the manufacturer! The 74HCT541 was required to match CMOS to TTL levels and will be useful for future plans (i.e., bidirectional data flow). In a later test, a 20Mhz clock chip and a ripple counter were used to generate a clock signal which was fed to pin5 of the 74HCT00. A slower output of the ripple counter was used as a faster test input to the HI1175.



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